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Implementation of 1.5 GHz Current Reusing Low Noise Amplifier for Ultra Narrow Band Applications

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Keywords

Low Noise Amplifier, CMOS, Noise figure, Radio Frequency, Interference, Receiver

In this paper the Low Noise Amplifier (LNA) operating with a centre frequency of 1.5 GHz is designed using 0.25µm CMOS technology. The Designed FB-LNA uses a stagger-tuning technique. A current-reused architecture is employed to decrease the power consumption using an input common-gate stage, common-gate low- noise amplifier (CGLNA) exhibits a relatively high noise figure (NF) at low operating frequencies. The technique also enables a significant reduction in current consumption. Designed LNA can be used for narrow band receiver applications.

Introduction

Narrow-Band low-noise amplifiers (LNAs) are used in receiving systems where the ratio between bandwidth (BW) and its center frequency fc can be as large as two. Application examples are analog cable (50–850 MHz), satellite (950–2150 MHz), and terrestrial digital (450–850MHz) video broadcasting. Moreover, a Narrow-band LNA can replace several LC-tuned LNAs typically used in multiband and multimode narrow-band receivers. A Narrow-band solution saves chip area and fits better with the trend towards flexible radios with as much signal processing (e.g., channel selection, image rejection, etc.) as possible in the digital domain (toward "software radio") [1]. CMOS technology is a satisfactory choice for the implementation of the low band UWB system when considering the time to market, hardware cost, the degree of difficulty, etc [2]. The UWB radio exhibits desirable features such as large transmission channel capacity, fine time and range resolution, less multipath fading effect and easier material penetration. Possible applications are high- data-rate wireless connection, high-accuracy positioning/locating, penetration imaging, etc. the need for ultra Narrowband (UWB) circuits is in steady rise for high data rate and multi-band applications [3]. Most reported full band UWB LNAs are implemented as a common- source or cascode topology, each of which provides acceptable gain and input matching while dissipating rather low power.

However, these common-source or cascode UWB LNAs tend to show unacceptably high noise figure (NF) cutoff frequency dependence [4]. UWB LNA which can provide nearly constant NF over the full frequency band of 1 -10 GHz [5].In a wireless receiver the information being transmitted is either data or voice which is used to change a radio frequency (RF) carrier. In RF front end design the first stage is a LNA. CMOS has become a competitive technology for radio transceiver implementation of various wireless communication systems due to high cut off frequency, higher level of integrability, lower cost, etc[6]. As the gain provided by the LNA increases the overall noise figure of the receiver reduces correspondingly. For a receiver high gain is required when the received signal is very weak. So the LNA has to provide high gain, good input and output matching and very low power consumption. Moreover, the differential topology improves the performance by providing better rejection of common mode noise, less sensitivity to substrate and power supply noise, improved power supply rejection ratio and higher linearity [7].

Design of Proposed LNA

The Low Noise Amplifier (LNA) operating with a centre frequency of 1.5 GHz is designed using 0.25µm CMOS technology. The Designed FB-LNA uses a stagger-tuning technique. A current-reused architecture is employed to decrease the power consumption using an input common-gate stage, common-gate low-noise amplifier (CGLNA) exhibits a relatively high noise figure (NF) at low operating frequencies. The technique also enables a significant reduction in current consumption. Designed

LNA can be used for narrow band receiver applications.

The Designed LNA is shown in Fig. 1. There are two stages including an input common-gate (CG) amplifier M1 and a common-source (CS) amplifier M2. The first stage provides an input impedance matching of 50Ω for RF signals from an antenna to LNA. The second stage acts as a gain stage, which assures that the weak RF signals will be greatly amplified. The first and second stages are constructed as cascode configurations to lower power consumption. The input impedance of M2 becomes an output load for M1 . An output buffer, recognized as a source follower M3 , is cascaded with the second stage. M4 is a current source, which provides a biasing current for M3.Cs and LS are part of the input matching network.C1 and L3 are ac coupling paths for signals into M2.R1 is added to supply a dc bias for M2. A high-frequency ac current into source of M2 flows to ground by adding the bypass-capacitor C2 , which avoids the signal interference coupling back to M1.C4 and L4 are part of the output matching network. The signal interference coupling back to M1. C4 and L4 part of the output matching network. The capacitor C1 provides a signal coupling path between M1 and M2. It is shown that two current biasing streams are required for M1 to match the input impedance and for to amplify the received signal. Large power consumption of such a CG-CS cascaded topology is inevitable.

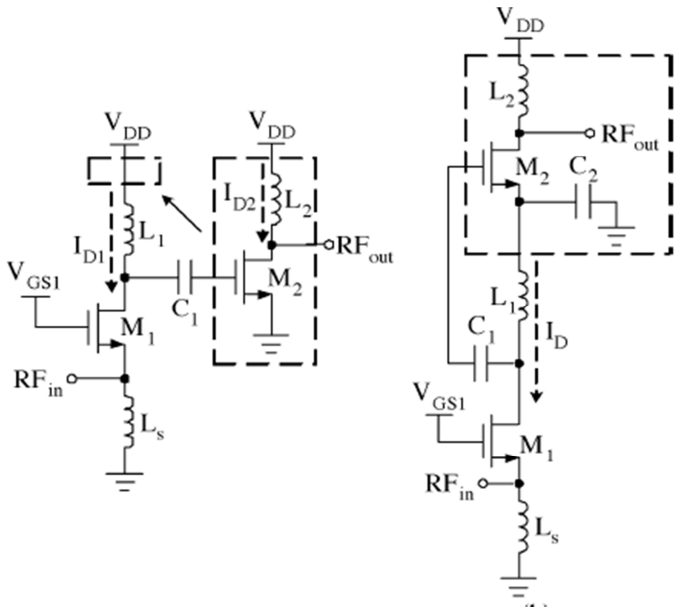

Fig 1. *Two-stage CG-CS amplifiers of: (a) cascaded topology, (b) Cascaded as current-reusing topology*

The differential amplification of the signal ensures reduction of the common mode signal, in most of the systems this common mode signal will be noise. Differential Low noise amplifier (DLNA) is designed using 0.25µm CMOS technology with a center frequency of 1.5 GHz and specification details are tabulated in Table 1. DLNA is designed with source degeneration configuration. The design is done using Advanced Design System. Fig. 2 shows the schematic of Differential Low Noise Amplifier design. The filter configuration can be used to extend the narrow band LNA to achieve the broadband operating property. The CS LNA is Narrowly used in narrow band application. The input impedance matching is achieved with the noiseless components. So it can achieve the lower NF. The narrowband LNA only can match to 50Ω in a single frequency rather than a Narrowband

The design specifications for Differential Low Noise Amplifier include center frequency, Channel Bandwidth, Length and width of the transistor. The gain and Noise figure plays an important role in Differential Low Noise Amplifier design. Gain is given by equation 1.

$$\text{Gain}=20*\log(\text{Vout}/\text{Vin}) \quad (1)$$

Noise is measured in terms of Noise Figure as a function of frequency. Noise figure is the measure of degradation of the Signal to Noise Ratio (SNR) caused by the component of Radio Frequency signal chain.

$$\text{Noise Figure (NF)} = \text{SNRi}/\text{SNRo} \quad (2)$$

Where SNRi is the SNR in dB at input of the Low Noise Amplifier and SNRo is the SNR in dB at the output of the Amplifier. A balun is used at the input to convert the single ended signal from the antenna to a differential ended signal. The simulation is done using Advanced Design System software.

Table I. *Design Specifications*

Parameter	Specification
Topology	LNA
Frequency	1500MHZ
Center Frequency	1.5GHZ
Channel Bandwidth	75 MHZ
Length	0.25u
Width	144u
DC Voltage	2v
Gain S21 (db)	450
S11 (db)	-3.5
LS	3.3nH
CS	3pF

Implementation of Current Reusing LNA

The Designed LNA is simulated with a 0.25-µm CMOS RF model. The performances of gain, input/output matching, power consumption, noise, and linearity are specified in order to regulate the values of the circuit components. The post-layout simulation results are provided at 2.0 V. The power gain is related to the reflection coefficients S11 is decided by the input matching condition. The output reflection coefficient S22 is adjusted by the source, figure 6.2 and 6.3 are the measured results of the input reflection coefficient S11 and the output reflection coefficient S22 respectively. These transmission zeros, which existed at 1.5 GHz for both S11 and S22, are caused by the series LC resonance of the parasitic inductance and capacitance. The measured results of both S11 and S22 are kept less than 10 dB within full band, which allows the transferring of RF signals and conform the UWB standard.

In order to achieve low-power consumption, Hence, the width of M1 is calculated to be 144 m. The width of M2 is 80 µm; to meet the linearity specification.L1 is chosen to resonate at 3 GHz with the parasitic capacitances, as well as the capacitance between the bottom plate of C1 and ground at the drain node of M1. Additionally, L2 of the second inter-stage is chosen to resonate at 11 GHz. The inductances of and are 9.7 and 3.3 nH, respectively.L3, implemented by a symmetric inductor, is 1.6 nH. Is selected to be 3.3 nH. Acts as a coupling capacitor, which is 2 pF.C2 is adjusted to 4 Pf in order to provide an ideal ac ground for M2 .R1 is 5.5 kΩ, which provides the bias voltage from VDD for M2. The output impedance is matched to 50Ω by a buffer stage for RF measurement purposes.

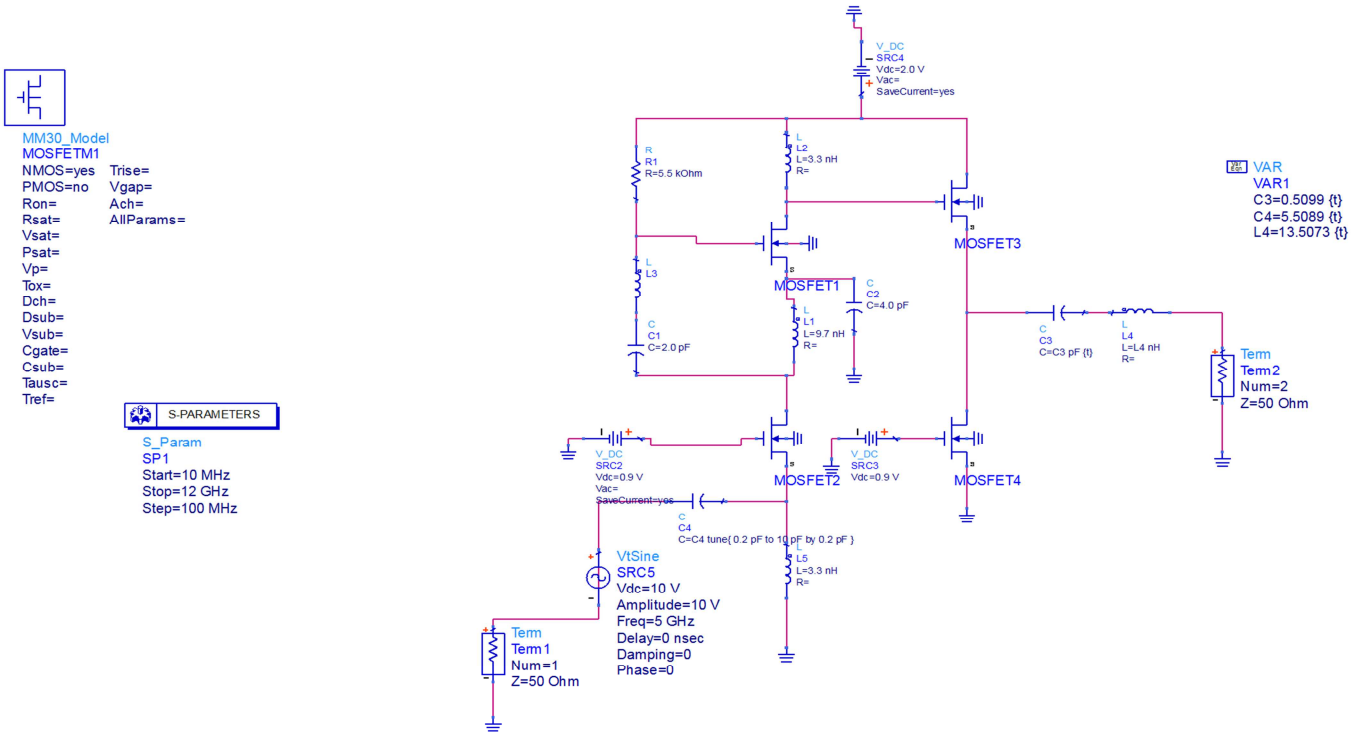

Fig. 2. *Implementation of designed current reusing-LNA including feedback and output buffers*

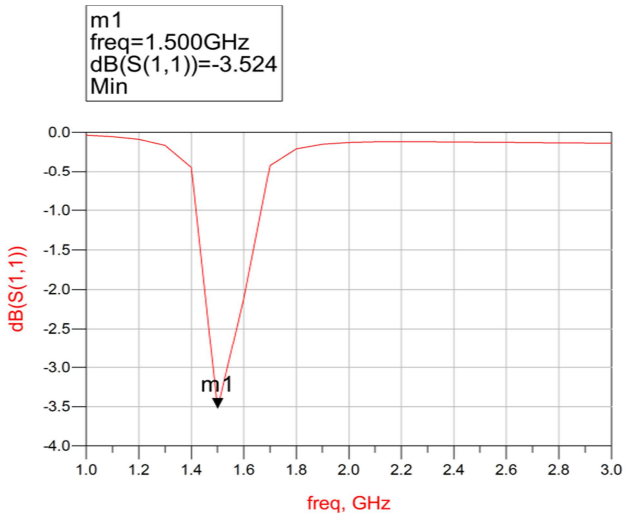

Fig 3. S-Parameter Simulations S1, 1 input reflection coefficient

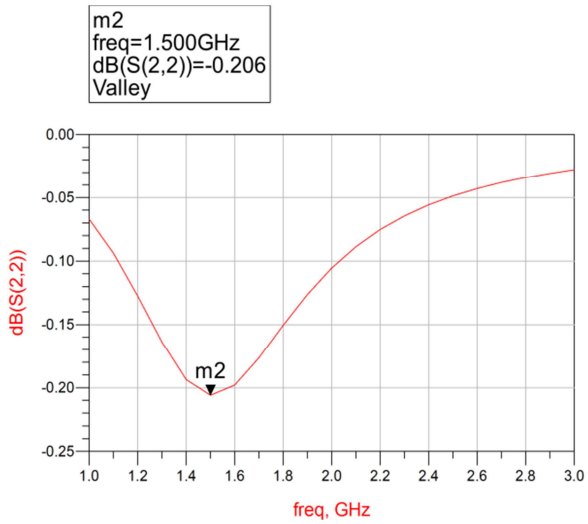

Fig 4. S-Parameter Simulations S2,2 output reflection coefficient

S-Parameter simulation is performed to find the return loss and stability factor. K greater than one implies the circuit is unconditionally stable for the designed frequency. Rolette Stability factor (K).

$$K=\frac{1+|\Delta|2-|S11|2-|S22|2}{2|S12\ S21|}+\cdots$$

$$\Delta=|S11S22-S12S21|<1$$

When K-factor is greater than one, the circuit will be unconditionally stable for any combinations of source and load impedance.

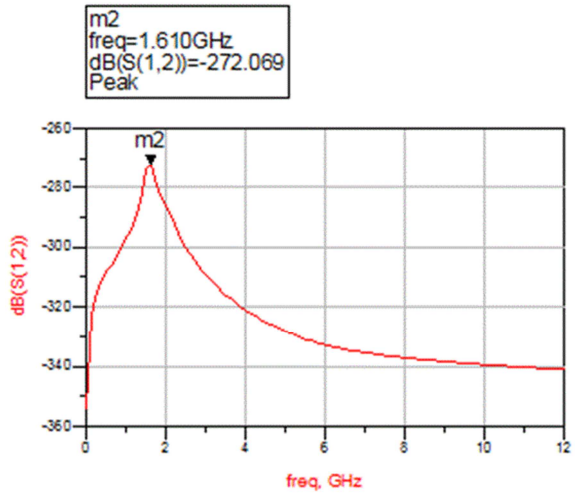

Fig 5. S-Parameter Simulation S1, 2 isolation

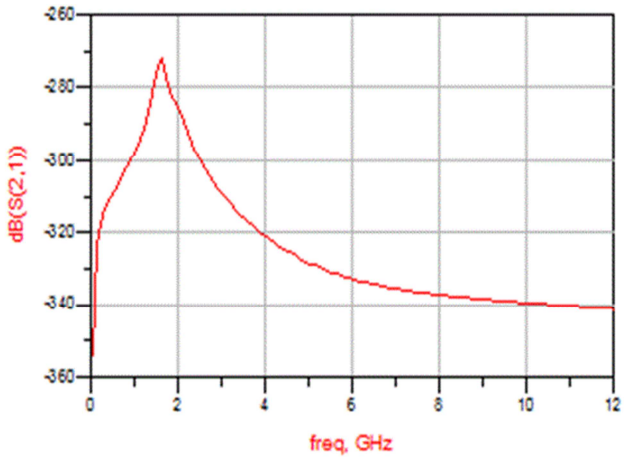

Fig 6. S-Parameter Simulation S 2, 1 power gain

In order to achieve low-power consumption, hence, the width of M1 is calculated to be 144 m. The width of M2 is 80 µm; to meet the linearity specification.L1 is chosen to resonate at 3 GHz with the parasitic capacitances, as well as the capacitance between the bottom plate of C1 and ground at the drain node of M1. Additionally, L2 of the second inter-stage is chosen to resonate at 1-12 GHz. The inductances of and are 9.7 and 3.3 nH, respectively.L3, implemented by a symmetric inductor, is 1.6 nH. Is selected to be 3.3 nH. Acts as a coupling capacitor, which is 2 pF.C2 is adjusted to 4 pF in order to provide an ideal ac ground for M2 .R1 is 5.5 kΩ, which provides the bias voltage from VDD for M2. The output impedance is matched to 50Ω by a buffer stage for RF measurement purposes.

Conclusion and Recommendations

A low-power FB Current Reusing-LNA for receiver front-ends in ultra narrow band systems is designed. The CG, cascoded to CS topology, provides a current-reuse technique to save the power consumption. Low Noise Amplifier is designed using 0.25µm CMOS technology for 1500MHz band wireless receiver. The design has been done using Advanced Design System Software. The designed Differential Low noise Amplifier provides a gain of -3.524bB. UWB systems with high-data-rate transmission and high-accuracy locating ability LNA to tune to particular frequency based on the applications such as the ISM Radios and GPS Receiver applications.■

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